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DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same (period or cycle or time)	216	L3
L2	L1 same slave same request$3	301	L2
L1	(bus adj1 (master or controller)) same arbit$6	2298	L1

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L4	L2 same (period or cycle or time)	0	L4
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	L2 same (period or cycle or time)	216	L3
L2	L1 same slave same request$3	301	L2
L1	(bus adj1 (master or controller)) same arbit$6	2298	L1

END OF SEARCH HISTORY

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(370/461 |370/462 |709/208 |709/253 |710/110 |710/107 |710/113 |710/309 |710/240).ccls.	2882

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	DB=USPT,USOC; PLUR=YES; OP=OR		
L5	710/110,107,113,309,240;709/208,253;370/461,462.ccls.	2882	L5
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L4	L2 same (period or cycle or time)	0	L4
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	L2 same (period or cycle or time)	216	L3
L2	L1 same slave same request$3	301	L2
L1	(bus adj1 (master or controller)) same arbit$6	2298	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L3 and L5	67

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IBM Technical Disclosure Bulletins

Search: L6

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Set Name side by side	Query	Hit Count	Set Name result set
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L6	l3 and L5	67	L6
L5	710/110,107,113,309,240;709/208,253;370/461,462.ccls.	2882	L5
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L4	L2 same (period or cycle or time)	0	L4
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	L2 same (period or cycle or time)	216	L3
L2	L1 same slave same request$3	301	L2
L1	(bus adj1 (master or controller)) same arbit$6	2298	L1

END OF SEARCH HISTORY

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  - L2: (67) l1 same slave sam
  - L3: (32) l2 same (period o
  - L4: (14) l3 same operat$3
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1	BRS	L1	372	(bus adj1 (master or controller)) same arbit$6	USPAT	2004/08/05 09:35			0
2	BRS	L2	67	l1 same slave same request$3	USPAT	2004/08/05 09:35			0
3	BRS	L3	32	l2 same (period or cycle or time)	USPAT	2004/08/05 09:38			0
4	BRS	L4	14	l3 same operat$3	USPAT	2004/08/05 09:39			0

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EAST - [Untitled1:1]

File View Edit Tools Window Help

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L2: (67) l1 same slave sam
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DBs USPAT

Plurals

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l3 same operat$3

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6772254 B2	20040803	19	Multi-master computer system with overlapped read and	710/110	710/113; 710/305
2	☐	☐	US 6216189 B1	20010410	11	Error master detector	710/113	714/43
3	☐	☐	US 5978879 A	19991102	23	Bus bridge apparatus	710/311	710/110
4	☐	☐	US 5923859 A	19990713	35	Dual arbiters for arbitrating access to a	710/113	710/114; 710/119;
5	☐	☐	US 5797020 A	19980818	24	Bus master arbitration circuitry having improved	710/240	710/107
6	☐	☐	US 5708794 A	19980113	8	Multi-purpose usage of transaction backoff and bus	711/154	710/108; 710/110;
7	☐	☐	US 5572734 A	19961105	20	Method and apparatus for locking arbitration on a	710/200	
8	☐	☐	US 5471590 A	19951128	23	Bus master arbitration circuitry having improved	710/108	340/825.5; 370/462;
9	☐	☐	US 5321819 A	19940614	31	Interface for coupling a host device having a network	709/228	709/230; 709/250
10	☐	☐	US 5305317 A	19940419	32	Local area network adaptive circuit for multiple network	370/257	370/469
11	☐	☐	US 5299193 A	19940329	31	Signal interface for coupling a network front end	370/463	370/465

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master and slave and arbit* and (period or time) Search

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1 **Scheduling strategies for master-slave tasking on heterogeneous processor platforms**
Banino, C.; Beaumont, O.; Carter, L.; Ferrante, J.; Legrand, A.; Robert, Y.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 15 , Issue: 4 , April 2004
Pages:319 - 330

[Abstract] [PDF Full-Text (859 KB)] **IEEE JNL**

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2 **Scheduling of low level computer vision algorithms on networks of heterogeneous machines**
Nolan, A.R.; Everding, B.; Wee, W.;
Computer Architectures for Machine Perception, 1995. Proceedings. CAMP '95 20 Sept. 1995
Pages:352 - 358

[Abstract] [PDF Full-Text (532 KB)] **IEEE CNF**

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3 **Logical timing (global synchronization of asynchronous arrays)**
Varshavsky, V.; Marakhovsky, V.; Tam-Anh Chu;
Parallel Algorithms/Architecture Synthesis, 1995. Proceedings. First Aizu International Symposium on , 15-17 March 1995
Pages:130 - 138

[Abstract] [PDF Full-Text (652 KB)] **IEEE CNF**

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4 **Concurrent round-robin-based dispatching schemes for Clos-netwoı switches**
Oki, E.; Zhigang Jing; Rojas-Cessa, R.; Chao, H.J.;
Networking, IEEE/ACM Transactions on , Volume: 10 , Issue: 6 , Dec. 2002

Pages:830 - 844

[Abstract] [PDF Full-Text (1468 KB)] **IEEE JNL**

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5 **Improvement of operation for tele-manipulation system using virtu reality: realization of common movement direction and common forcε direction in master and slave at arbitrary viewpoint**
Tsuge, H.; Fukuda, T.; Arai, F.; Inaba, A.; Niwa, Y.;
Industrial Electronics Society, 2000. IECON 2000. 26th Annual Confjerence ol IEEE , Volume: 2 , 22-28 Oct. 2000
Pages:948 - 953 vol.2

[Abstract] [PDF Full-Text (483 KB)] **IEEE CNF**

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6 **A robust differential scan flip-flop**
Vesterbacka, M.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Interna Symposium on , Volume: 1 , 30 May-2 June 1999
Pages:334 - 337 vol.1

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

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7 **Stability guaranteed teleoperation: an adaptive motion/force contr approach**
Wen-Hong Zhu; Salcudean, S.E.;
Automatic Control, IEEE Transactions on , Volume: 45 , Issue: 11 , Nov. 200(
Pages:1951 - 1969

[Abstract] [PDF Full-Text (516 KB)] **IEEE JNL**

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8 **Bilateral telemanipulator system with communication time delay ba on force-sum-driven virtual internal models**
Otsuka, M.; Matsumoto, N.; Idogaki, T.; Kosuge, K.; Itoh, T.;
Robotics and Automation, 1995. Proceedings., 1995 IEEE International Confe on , Volume: 1 , 21-27 May 1995
Pages:344 - 350 vol.1

[Abstract] [PDF Full-Text (776 KB)] **IEEE CNF**

Scheduling strategies for master-slave tasking on heterogeneous processor platforms

Banino, C. Beaumont, O. Carter, L. Ferrante, J. Legrand, A. Robert, Y.
LaBRI, CNRS, Talence, France

This paper appears in: **Parallel and Distributed Systems, IEEE Transacti**

Publication Date: April 2004
On page(s): 319 - 330
Volume: 15 , Issue: 4
ISSN: 1045-9219
Inspec Accession Number: 7951830

Abstract:
We consider the problem of allocating a large number of independent, equal-s to a heterogeneous computing platform. We use a nonoriented graph to mode platform, where resources can have different speeds of computation and com Because the number of tasks is large, we focus on the question of determinin optimal steady state scheduling strategy for each processor (the fraction of **ti** computing and the fraction of **time** spent communicating with each neighbor) contrast to minimizing the total execution **time**, which is NP-hard in most for we show that finding the optimal steady state can be solved using a linear pr approach and, thus, in polynomial **time**. Our result holds for a quite general f allowing for cycles and multiple paths in the interconnection graph, and allowi several **masters**. We also consider the simpler case where the platform is a t this case can also be solved via linear programming, we show how to derive a form formula to compute the optimal steady state, which gives rise to a band centric scheduling strategy. The advantage of this approach is that it can dire autonomous task scheduling based only on information local to each node; nc information is needed. Finally, we provide a theoretical comparison of the con power of tree-based versus **arbitrary** platforms.

Index Terms:
computational complexity linear programming optimisation processor scheduling tre (mathematics) NP-hard problem bandwidth centric scheduling strategy heterogeneou platform linear programming approach **master slave** tasking optimal steady state

Documents that cite this document

L9: Entry 2 of 19 File: USPT May 18, 2004

DOCUMENT-IDENTIFIER: US 6738845 B1
TITLE: Bus architecture and shared bus arbitration method for a communication device

Current US Original Classification (1):
710/240

Current US Cross Reference Classification (1):
710/110

CLAIMS:

21. A system, comprising: a first data processing subsystem comprising a first processor coupled to a first bus as a first bus master; a second data processing subsystem comprising a second processor coupled to a second bus as a second bus master; a first slave subsystem comprising a memory unit coupled to a third bus; a second slave subsystem comprising a fourth bus; and a bus arbitration module (BAM), having the first, second, third, and fourth busses coupled thereto, configured and arranged to couple each of the third and fourth busses to any selected one of at least the first and second busses so that each of first and second slave subsystems can be independently accessed by either of the first and second data processing subsystems, thereby enabling the first and second data processing subsystems to access different ones of the first and second slave subsystems at the same time, the BAM being further configured and arranged to employ an arbitration scheme for access to at least a first one of the first and second slave subsystems in which, during any period when all requests for access to the first one of the first and second slave subsystems are of the same priority level, a first one of the first and second data processing subsystems is guaranteed to have access to a greater portion of the available bandwidth of the first one of the first and second slave subsystems than is a second one of the first and second data processing subsystems.

L9: Entry 2 of 19 File: USPT May 18, 2004

US-PAT-NO: 6738845
DOCUMENT-IDENTIFIER: US 6738845 B1

TITLE: Bus architecture and shared bus arbitration method for a communication device

DATE-ISSUED: May 18, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hadwiger; Rainer R.	North Andover	MA		
Krivacek; Paul D.	Cambridge	MA		
S.o slashed.rensen; J.o slashed.rn	Aars			DK
Birk; Palle	Gistrup			DK

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Analog Devices, Inc.	Norwood	MA			02

APPL-NO: 09/ 706577 [PALM]
DATE FILED: November 3, 2000

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application claims domestic priority under 35 U.S.C. .sctn.119(e) to U.S. Provisional Patent Application Serial No. 60/163,816, filed Nov. 5, 1999, now abandoned, and incorporated herein in its entirety by reference.

INT-CL: [07] G06 F 13/38

US-CL-ISSUED: 710/240; 710/241, 710/244, 710/306, 710/308, 710/316, 710/317, 710/110, 710/305
US-CL-CURRENT: 710/240; 710/110, 710/241, 710/244, 710/305, 710/306, 710/308, 710/316, 710/317

FIELD-OF-SEARCH: 710/240, 710/241, 710/244, 710/306, 710/308, 710/316, 710/315, 710/317, 710/110, 710/305, 713/600, 370/366, 709/209, 709/210, 703/28

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

☐	4276594	June 1981	Morley	713/600
☐	4639910	January 1987	Toegel et al.	370/366
☐	4698753	October 1987	Hubbins et al.	709/209
☐	5278974	January 1994	Lemmon et al.	713/600
☐	5467295	November 1995	Young et al.	709/210
☐	5539882	July 1996	Gopal et al.	709/220
☐	5627976	May 1997	McFarland et al.	710/309
☐	5634004	May 1997	Gopinath et al.	710/317
☐	5649209	July 1997	Umetsu et al.	710/266
☐	5649233	July 1997	Chen	710/8
☐	5734848	March 1998	Gates et al.	710/315
☐	5754780	May 1998	Asakawa et al.	709/208
☐	5909559	June 1999	So	395/307
☐	5931931	August 1999	Nguyen	710/113
☐	5987549	November 1999	Hagersten et al.	710/107
☐	6006303	December 1999	Barnaby et al.	710/244
☐	6026461	February 2000	Baxter et al.	
☐	6038630	March 2000	Foster et al.	710/132
☐	6047349	April 2000	Klein	710/129
☐	6061361	May 2000	An et al.	370/462
☐	6070205	May 2000	Kato et al.	710/100
☐	6223230	April 2001	Garnett et al.	710/26
☐	6347294	February 2002	Booker et al.	703/28
☐	6363453	March 2002	Esposito et al.	711/2
☐	6389493	May 2002	Barkley et al.	710/110
☐	6496740	December 2002	Robertson et al.	700/20
☐	6496890	December 2002	Azevedo et al.	710/110
☐	6519666	February 2003	Azevedo et al.	710/120
☐	6671761	December 2003	Kim	710/244

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0426413	May 1991	EP	
0702307	March 1996	EP	
0924623	June 1999	EP	
WO 99/26155	May 1999	WO	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ASSISTANT-EXAMINER: King; Justin

ATTY-AGENT-FIRM: Wolf, Greenfield & Sacks, P.C.

ABSTRACT:

A multiple bus architecture includes multiple processors, and one or more shared peripherals such as memory. The architecture includes plural bus masters, each connected to its own bus. There are also plural bus slaves, each connected to its own bus. A bus arbitration module selectively interconnects the buses, so that when the plural bus masters each access a different bus slave, no blocking occurs, and when the plural bus masers each access a same bus slave, bandwidth starvation is avoided. The architecture is supported by a bus arbitration method including hierarchical application of an interrupt-based method, an assigned slot rotation method and a round-robin method, which avoids both bandwidth starvation and lockout during extended periods of bus contention.

25 Claims, 4 Drawing figures

Previous Doc Next Doc Go to Doc#

L9: Entry 4 of 19 File: USPT Jan 9, 2001

US-PAT-NO: 6173349
DOCUMENT-IDENTIFIER: US 6173349 B1

TITLE: Shared bus system with transaction and destination ID

DATE-ISSUED: January 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Qureshi; Amjad Z.	San Jose	CA		
Nguyen; Le Trong	Monte Sereno	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Samsung Electronics Co., Ltd.	Kyungki-do			KR	03

APPL-NO: 08/ 731393 [PALM]
DATE FILED: October 18, 1996

INT-CL: [07] G06 F 13/36

US-CL-ISSUED: 710/110; 710/113, 710/107, 710/240, 710/241
US-CL-CURRENT: 710/110; 710/107, 710/113, 710/240, 710/241

FIELD-OF-SEARCH: 395/290, 395/291, 395/293, 395/296, 395/298, 395/299, 395/728, 395/729, 395/731, 395/840, 395/841, 395/284, 395/287

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5418967	May 1995	Simcoe et al.	395/726
5475850	December 1995	Kahn	395/290
5506971	April 1996	Gullette et al.	395/296
5533204	July 1996	Tipley	395/288
5535363	July 1996	Prince	711/147
5574849	November 1996	Sonnier et al.	714/12
5574868	November 1996	Marisetty	395/298

☐	5613075	March 1997	Wade et al.	395/287
☐	5649209	July 1997	Umetsu et al.	395/739
☐	5737546	April 1998	Fenwick et al.	395/290
☐	5802055	September 1998	Krein et al.	370/402
☐	5835739	November 1998	Bell et al.	710/128
☐	5925120	July 1999	Arp et al.	710/131
☐	5937171	August 1999	Sarangdhar et al.	710/105
☐	5941973	August 1999	Kondo et al.	710/129

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Phan; Raymond N

ATTY-AGENT-FIRM: Skjerven Morrill MacPherson LLP Millers; David T.

ABSTRACT:

To reduce latency on a shared bus during bus arbitration, a novel shared bus system uses device select lines between a bus arbiter and the bus devices to select the bus slave concurrently with the granting of the shared bus to the bus master. Specifically, a bus device requests the use of the shared bus by driving an active state on a bus request terminal and driving a destination ID value corresponding to the desired bus slave to the bus arbiter. The bus arbiter then drives an active state on a bus grant output terminal coupled to the bus grant input terminal of the requesting device. Concurrently, the bus arbiter drives an active state on the device select output terminal coupled to the device select input terminal of the desired bus slave. In addition posted read request tagging can be simplified using a transaction ID bus to supplement the shared bus.

13 Claims, 8 Drawing figures

Previous Doc Next Doc Go to Doc#

L9: Entry 7 of 19 File: USPT Jul 13, 1999

DOCUMENT-IDENTIFIER: US 5923859 A
TITLE: Dual arbiters for arbitrating access to a first and second bus in a computer system having bus masters on each bus

Detailed Description Text (21):
The OWNER[6:0] and LOCKED[6:0] signals and the CUT.sub.-- RETRY.sub.-- MSTR signal are provided to the CUT mask generation logic 452, which also receives a signal referred to as the CUT.sub.-- RETRY.sub.-- MSK.sub.-- EN or cut retry mask enable signal from a bit in an arbitrary I/O port. This bit is used to enable or disable operation of the feature wherein the bus request signal of a requesting bus master which has been retried based on an access to the PCI-EISA bridge 130 is masked until the cycle can be completed without a further retry. When this feature is disabled, which is not preferable, then the master may repeatedly retry prior to the data being available. The output of the CUT mask generation logic 452 is the CUT.sub.-- MSK[6:0] signals. Further details of the logic are provided in FIG. 6. The OWNER[x] and !LOCKED[x] signals are the inputs to a two-input AND gate 454. The output of the AND gate 454 is connected to the D input of a D-type flip-flop 456. The non-inverted output of the flip-flop 456 is the CUT.sub.-- MSK[x] signal. The clocking signal to the flip-flop 456 is provided by the output of a two-input OR gate 458 which receives the CUT.sub.-- RETRY.sub.-- MSTR signal at one input and the output of a three-input OR gate 460 at its second input. The output of the OR gate 460 is also provided to the clear input of the flip-flop 456. The OR gate 460 receives the PCI.sub.-- RESET, !RETRY and !CUT.sub.-- RETRY.sub.-- MSK.sub.-- EN signals. The RETRY signal is provided under several conditions. First, a cycle is directed to the EISA bus E, but another cycle is already in progress on the EISA bus E. One example is when a prior master has posted a write operation to the EISA bus E and that write operation is occurring. Second, a cycle is directed to the EISA bus E when a refresh cycle on the EISA bus E is pending or is in progress. The third condition is when the PCI-EISA bridge 130 is the responding PCI slave, a lock has been set and the requesting bus master is not the locking bus master. This condition occurs as the PCI-EISA bridge 130 must not execute a cycle as a locked resource to any master except the one placing the lock. The RETRY signal is asserted when any of these events occur and is removed or negated when the assertion event is completed, such as the lock being released, the posted write completing or the refresh completing. The PCI-EISA bridge 130 can obviously determine when it is unlocked and can determine the other two events as it is performing the posted write operation and it includes the refresh controller. Therefore if a cycle directed to the PCI-EISA bridge 130 is retried, and the PCI-EISA bridge 130 is not locked, then the CUT.sub.-- MSK bit is set to allow this master's bus request to be masked until the retry source event is completed.

Current US Original Classification (1):
710/113

Current US Cross Reference Classification (4):
710/240

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L9: Entry 7 of 19 File: USPT Jul 13, 1999

US-PAT-NO: 5923859
DOCUMENT-IDENTIFIER: US 5923859 A

TITLE: Dual arbiters for arbitrating access to a first and second bus in a computer system having bus masters on each bus

DATE-ISSUED: July 13, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Melo; Maria L.	Houston	TX		
Lester; Robert Allan	Houston	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Compaq Computer Corporation	Houston	TX			02

APPL-NO: 08/ 974149 [PALM]
DATE FILED: November 19, 1997

PARENT-CASE:
This is a continuation of application Ser. No. 08/421,202, filed on Apr. 13, 1995 now abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/293; 395/294, 395/299, 395/728, 395/726
US-CL-CURRENT: 710/113; 710/114, 710/119, 710/200, 710/240

FIELD-OF-SEARCH: 395/293, 395/294, 395/299, 395/726, 395/728

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4755938	July 1988	Takahashi et al.	
4980854	December 1990	Donaldson et al.	
4987529	January 1991	Craft et al.	364/200
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☐	5083260	January 1992	Tsuchiya	395/325
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Peripheral Components, Intel Corp., pp. 1-215, 1-222 to 1-225, 1-245 to 1-246, 1-265 to 1-267, 1-280 to 1-285 (1993).

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Thlang; Eric S.

ATTY-AGENT-FIRM: Akin, Gump, Strauss, Hauer & Feld, L.L.P.

ABSTRACT:

Arbitration circuitry in a computer system having a plurality of arbiters for arbitrating requests from bus masters on a PCI bus and an EISA bus. Each of the PCI and EISA buses have a plurality of masters. The PCI bus utilizes a modified LRU arbitration scheme, while the EISA bus utilizes a rotating priority scheme. The arbiter on the EISA bus includes a first level of arbitration and a second level of arbitration. The first level is assigned a plurality of requester types to determine the priority between the requestor types. Certain of the first level requestor types include a plurality of devices. If one of those certain requestor types wins priority on the first level arbitration cycle, a second level

arbitration is performed to determine the priority between the plurality of devices.

32 Claims, 20 Drawing figures

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L9: Entry 12 of 19 File: USPT Jul 15, 1997

US-PAT-NO: 5649209
DOCUMENT-IDENTIFIER: US 5649209 A

TITLE: Bus coupling information processing system for multiple access to system bus

DATE-ISSUED: July 15, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Umetsu; Masakazu	Tokyo			JP
Katagiri; Masami	Yamagata			JP
Hoshizawa; Yoshihiro	Yamagata			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NEC Corporation	Tokyo			JP	03

APPL-NO: 08/ 713289 [PALM]
DATE FILED: September 10, 1996

PARENT-CASE:
This application is a continuation of application Ser. No. 08/187,542, filed Jan. 28, 1994, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	5-014184	January 29, 1993

INT-CL: [06] G06 F 12/00

US-CL-ISSUED: 395/739; 395/868, 395/741, 395/306
US-CL-CURRENT: 710/266; 710/110, 710/268, 710/309, 710/48

FIELD-OF-SEARCH: 395/868, 395/730, 395/739, 395/741, 395/306

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	5001625	March 1991	Thomas et al.	395/325
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☐	5539917	July 1996	Jirgal	395/842
☐	5555420	September 1996	Sarangdhar et al.	395/739

ART-UNIT: 235

PRIMARY-EXAMINER: Ray; Gopal C.

ASSISTANT-EXAMINER: Seto; Jeffrey K.

ATTY-AGENT-FIRM: Foley & Lardner

ABSTRACT:

When a first bus master device issues a bus request on a first request signal line, a centralized arbitration circuit in a system bus manage circuit issues a bus grant signal on a first grant signal line if the bus is available for use. This causes the first bus master device having gained the ownership of the bus to issue a read request to a first slave device. At this time a first signal line is designated. Even before the sending of the read data constituting a response to this read request to the first bus master device, a bus request from a second bus master device can be accepted if the data bus is unoccupied. Thus, the centralized arbitration circuit in the system bus manage circuit issues a grant signal on a second grant signal line. This causes the second bus master device having gained the ownership of the bus to designate a second end signal line, and to issue a read request to a second slave device. After that, the first end signal line is activated, and read data from the first slave device is sent to the first bus master device. On the other hand, the second end signal line is activated, and read data from the second slave device is sent to the second bus master device.

5 Claims, 5 Drawing figures

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US-PAT-NO: 5978879

DOCUMENT-IDENTIFIER: US 5978879 A

TITLE: Bus bridge apparatus

---------- KWIC ---------

Brief Summary Text - BSTX (20):

When, by an access as a slave device by a master device on a second system bus for accessing a slave device on a first system bus, the apparatus issues a bus acquisition request to an arbiter on the first system bus for serving as a bus master of the first system bus so that time-out is likely to occur on the second system bus before acquiring the right to use the first system bus, this bus bridge apparatus performs functions: (i) on the second system bus, issuing a resending request to the master device to terminate a bus cycle temporarily; (ii) on the first system bus, if it is before the apparatus acquires the right to use the first system bus, abandoning the bus acquisition request and, if it is after acquiring the right, delaying the cycle start operation while retaining the bus use right, by using said bus cycle generating means, thereafter; and (iii) starting the cycle for accessing a slave device on the first system bus if, before the bus use right is taken by an arbiter on the first system bus, a master device on the second system bus attempts to access the apparatus for accessing a slave device on the first system bus.

Brief Summary Text - BSTX (26):

When, by an access as a slave device by a master device on a second system bus for accessing a slave device on a first system bus, the apparatus issues a bus acquisition request to an arbiter on the first system bus for serving as a bus master of the first system bus so that time-out is likely to occur on the second system bus before acquiring the right to use the first system bus, this bus bridge apparatus performs functions: (i) on the second system bus, issuing a resending request to the first master device to terminate a bus cycle temporarily, and storing that the resending request was issued to the first master device, in said storing means; (ii) on the first system bus, issuing a bus acquisition request until the acquisition of the right to use the first system bus, and delaying the cycle while retaining the bus use right, by said bus cycle generating means, thereafter; (iii) if the bus use right is taken by

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US005978879A

United States Patent [19]

Harumoto et al.

[11] **Patent Number: 5,978,879**

[45] **Date of Patent: Nov. 2, 1999**

[54] **BUS BRIDGE APPARATUS**

[75] Inventors: **Hideaki Harumoto**, Moriguchishi; **Toshiyuki Ochiai**, Ibaraki; **Taihei Yugawa**, Narashi, all of Japan

[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Japan

[21] Appl. No.: **08/877,208**

[22] Filed: **Jun. 17, 1997**

[30] **Foreign Application Priority Data**

Jun. 18, 1996 [JP] Japan 8-156781

[51] **Int. Cl.^{6}** **G06F 13/00**

[52] **U.S. Cl.** **710/129; 710/110**

[58] **Field of Search** **395/306, 308, 395/309, 290; 710/110, 126, 128, 129**

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Primary Examiner—Glenn A. Auve
Attorney, Agent, or Firm—Parkhurst & Wendel, L.L.P.

[57] **ABSTRACT**

A bus bridge apparatus that connects two system buses independent of each other to which a bus arbiter operating independently and located outside of the apparatus, has a function for serving as a master and a slave of the system buses, a base address holding means, and a bus address generating means. When, to access a slave device on a first system bus, a master device on a second system bus attempts to access the apparatus, generating offset from addresses received from the master device and combining the offset with base addresses previously stored in said base address holding means, to generate an access destination address in the slave device by using said bus address generating means, this bus bridge apparatus performs functions: (i) issuing the generated access destination address by serving as a bus master on the first system bus, to access the slave device; and (ii) performing data transfer between the master device and the slave device by serving as a slave of the master device on the second system bus. It is thus possible to realize mutual access between system buses having an independent arbitration function, without changing system design.

1 Claim, 12 Drawing Sheets